**UNITED STATES DEPARTMENT OF COMMERCE**
**Patent and Trademark Office**
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. |
|---|---|---|---|
| 09/434,736 | 11/02/99 | KIM S | 000939-07360 |

020350 MM42/0309
TOWNSEND AND TOWNSEND AND CREW LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO CA 94111

| EXAMINER | |
|---|---|
| PERT,E | |
| **ART UNIT** | **PAPER NUMBER** |
| 2813 | |

**DATE MAILED:** 03/09/00

**Please find below and/or attached an Office communication concerning this application or proceeding.**

**Commissioner of Patents and Trademarks**

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/434,736 | KIM ET AL. | |
| | Examiner | Art Unit | |
| | Evan T. Pert | 2813 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

**Status**

1)☒ Responsive to communication(s) filed on *02 November 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-88* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,2 and 4* is/are allowed.

6)☒ Claim(s) *5-88* is/are rejected.

7)☒ Claim(s) *3* is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 November 1999* is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. § 119**

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☒ All b)☐ Some * c)☐ None of the CERTIFIED copies of the priority documents have been:

1.☐ received.

2.☒ received in Application No. (Series Code / Serial Number) *08/327,887* .

3.☐ received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

**Attachment(s)**

14) ☒ Notice of References Cited (PTO-892)
15) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
16) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
17) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
18) ☐ Notice of Informal Patent Application (PTO-152)
19) ☐ Other: .

## DETAILED ACTION

### *Reissue Applications*

1. The original patent, or an affidavit or declaration as to loss or inaccessibility of the original patent, must be received before this reissue application can be allowed. See 37 CFR 1.178.

2. This application is objected to under 37 CFR 1.172(a) as the assignee has not established its ownership interest in the patent for which reissue is being requested. An assignee must establish its ownership interest *in order to support the consent to a reissue application required by 37 CFR 1.172*(a). The submission establishing the ownership interest of the assignee is informal. There is no indication of record that the party who signed the submission (D. S. Chung) is an appropriate party to sign on behalf of the assignee. 37 CFR 3.73(b).

A proper submission establishing ownership interest in the patent, pursuant to 37 CFR 1.172(a), is required in response to this action.

The person who signed the submission establishing ownership interest is not recognized as an officer of the assignee (since the title "Director" alone is insufficient) , and he/she has not been established as being authorized to act on behalf of the assignee. See MPEP § 324.

It would be acceptable for a person, other than a recognized officer, to execute a submission establishing ownership interest, provided the record for the application

includes a statement that the person is empowered to sign a submission establishing ownership interest and/or act on behalf of the organization.

Accordingly, a new submission establishing ownership interest which includes such a statement above, will be considered to be executed by an appropriate official of the assignee. A separately filed paper referencing the previously filed submission establishing ownership interest and containing a proper empowerment statement would also be acceptable.

Applicant is also referred to page 1400-21 of the MPEP for an example of acceptable format shown as Form PTO/SB/54 (12-97).

3. Applicant is reminded of the continuing obligation under 37 CFR 1.56 to timely apprise the Office of any litigation information, or other prior or concurrent proceeding, involving Patent No. 5,683,938, which is material to patentability of the claims under consideration in this reissue application. This obligation rests with each individual associated with the filing and prosecution of this application for reissue. See MPEP §§ 1404, 1442.01 and 1442.04.

***Claim Objections***

4. Claim 3 is objected to because of the following informalities: On line 2 "contacts" should read --contact--. Appropriate correction is required.

***Examiner's Matrix of Claim Limitations***

5. Applicant has presented 22 pages of 83 new claims to add to the 5 claims of the originally issued patent to correct certain errors. Since the lengthy wording of these claims is cumbersome for claim analysis, the examiner, in an attempt to clarify the record, has provided a matrix of limitations vs. claims containing those limitations, attached as an appendix to this communication. By examining the matrix, rather than the claims directly, one can more easily compare claims along with their collective limitations.

In the matrix of the attached appendix, each numbered row represents a limitation presented in the original prosecution or in the new claims presented for reissue. Each numbered column represents an independent claim number. Within the matrix at (row, column) positions, an "x" indicates that the corresponding row limitation is present in the independent claim at the heading of the corresponding column. A numeral at a (row, column) location indicates dependent claim(s) that include the limitation of the corresponding row (and also include the "x" limitations of the corresponding column by dependence). Finally, a blank at a (row, column) position in the matrix means that the row's limitation is not present in either the independent claim at the heading of the column, nor in any claim depending from it.

***Examiner's Summary of Invention***

6. It is worthwhile, for clarification of the record, to present a summary of the invention from the examiner's perspective. The invention of the active patent is directed to a method of filling vias as applied to a multi-level wiring of semiconductor manufacturing. Key elements of the invention include: 1) a first insulating layer with first openings (having a tapered upper portion) in which metal is deposited followed by 2) a second layer with second openings over the first openings to extend the vias of the first layer and to create vias to circuit nodes that reside on the top of the first layer. The "two-step" deposition, that is one step for each layer, leads to improved more even via filling without problems found in the prior art.

Thus, in accordance with the patented invention, there is at least a "two-step" deposition as in the title of the patent wherein step 1 is the filling of a first layer and step 2 is a filling of a second, or subsequent, layer. Also key to the invention is that the filling is selective. That is, in making a selective deposition, examiner takes note that material is deposited selectively in the via, and not on the surface of the insulating layer having holes.

The distinction between a selective deposition and a blanket deposition with subsequent etch is important in understanding the practice of the invention, since, as explained in the background art of the patent:

> In the case of filling the contact holes with the highest surface topography with the selective tungsten thin films, the films become overgrown at the contact holes with rather lower surface topography and circuit failure may result between the metal wires (column 1, lines 27-31, emphasis added).

As explained by applicant, the filling holes of different depths by selective deposition results in overfilling of the shallowest hole first since, during selective deposition, the rate of growth is about equal in all of the holes. In a blanket deposition with patterning (such as that shown in the record by Tadahiko Tanaka in Fig. 4 of JP56-165320(A)), one is not concerned with overgrowth out of the hole since the layer is subsequently patterned anyway.

The present invention then, is clearly directed to multi-level wiring with selective deposition of conductive vias. The exact nature of selective deposition is not disclosed in the specification except that the selective deposition of tungsten is the preferred embodiment (col. 3, lines 36-38). Details for enablement of the selective deposition of tungsten is not disclosed, but many forms of selective deposition of metal were well known in the art at the time the invention was made, all such methods requiring some changing of parameters during "the step" of selective deposition. The state-of-the-art at the time is evidenced by, for example, the teachings of Smith et al., Wilson et al., Tobin, King et al., Stoll et al., and Chang & Wang, herein incorporated by reference on the Form PTO 892 included with this Office Action).

For example, Chang & Wang in their published European Patent Application give extensive details of selective deposition of tungsten on silicon in col. 3.

***Examiner's Summary of Corrections in Reissue***

7. Applicant has indicated:

> One error of the original patent corrected by the present reissue application is that the independent claims of the original patent require the deposition of metal layers, whereas those skilled in the art at the time of the invention would realize that the present invention equally applies to the deposition of other conductive layers, such as polysilicon. (3rd paragraph of reissue declaration).

This correction, specifically noted by applicant as being required, is presented in the claims corresponding to the blanks and numerals in rows 23, 39, 42, 47, 56, and 57 of the matrix of the attached appendix (matrix is explained under item 4 of this Office Action).

Examiner acknowledges and notes the following additional alterations (corrections evident from the matrix) that could be considered to affect patentability:

a. Preambles were changed per rows 2-5 of the matrix in the attached appendix. These changes re-word the "two-step" deposition, clarify that the method is intended for a semiconductor substrate, and that the material deposited is "conductive" rather than the more restrictive "metal" of the original preamble. Examiner notes that removal of "two-step" makes unclear how each deposition in each layer takes place. Applicant has argued a defining point to be the "number of steps" at each deposition (see item 3 of this Office Action).

b. Silicon substrate broadened to any substrate (row 6 of matrix).

c. Via connection layout is re-defined in various ways (rows 8-18, 27-31, and 34-38 of matrix). Examiner notes that these limitation changes do not differ over admitted prior art presented in applicant's "background of invention." That is to say, the present invention could be claimed by defining "nodes at the wafer surface" along with "nodes on the 1st insulating layer." The two-step deposition, then, is a step 1 where connections to the "nodes on the wafer surface" are made and a step 2 where connections to the filled vias in the 1st layer are made along with connections to "nodes on the 1st insulating layer."

d. Geometry of 1st contact holes broadened to be of unequal depth (row 19 of matrix).

e. Geometry of 1st contact holes broadened to not require tapered upper portion (row 20 of matrix).

f. Removed certain "defining" limitations which are inherent or optional to practice of the invention (rows 24, 25, and 26 of matrix).

g. Added forming "a second conductive pattern" (row 28 of matrix), which is not an addition since this polysilicon line is already anticipated (Ref 7 of patent).

h. Added dependent claims with fill by "CVD" - this limitation was present as dependent claims 2 and 7 of the original patent as applied to metal, but is now specified for deposition of any "conductive material" (as claims 57, 63, 82, and 88).

i. Added defining limitations as dependent claims corresponding to rows 42-46 and 48-55. Examiner takes notice that the limitations corresponding to these rows of the matrix are obvious variants of the admitted prior art.

***Drawings***

8. The drawings are objected to because of non-compliance with 37 CFR 1.84 as indicated by the Form PTO 948 included with this Office Action. Correction is required.

***Specification***

9. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

The following is a quotation of 37 CFR 1.71(a)-(c):

> (a) The specification must include a written description of the invention or discovery and of the manner and process of making and using the same, and is required to be in such full, clear, concise, and exact terms as to enable any person skilled in the art or science to which the invention or discovery appertains, or with which it is most nearly connected, to make and use the same.
>
> (b) The specification must set forth the precise invention for which a patent is solicited, in such manner as to distinguish it from other inventions and from what is old. It must describe completely a specific embodiment of the process, machine, manufacture, composition of matter or improvement invented, and must explain the mode of operation or principle whenever applicable. The best mode contemplated by the inventor of carrying out his invention must be set forth.
>
> (c) In the case of an improvement, the specification must particularly point out the part or parts of the process, machine, manufacture, or composition of matter to which the improvement relates, and the description should be confined to the specific improvement and to such parts as necessarily cooperate with it or as may be necessary to a complete understanding or description of it.

- The specification is objected to under 37 CFR 1.71 because it does not a support enablement of "filling a ... metal layer .. into ... holes ... by one single step" (claim 5).

- The specification is objected to under 37 CFR 1.71 because it does not support or provide a method for a "one step" selective deposition of polysilicon.

- The specification is objected to under 37 CFR 1.71 because it does not support a means to selectively deposit on other than a silicon substrate, noting that a selective deposition of tungsten on silicon at the time of the invention was well known.

- The specification is objected to under 37 CFR 1.71 because it fails to enable forming holes "by a CVD process" (as in claims 82 and 88).

***Claim Rejections - 35 USC § 112***

10. Claims 5-88 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

- Claim 5 limits the deposition to occur "by one single step", the method of which is not explained anywhere in the specification.

- Claims 44 and 71 provide that the first material filled into the first plurality of holes is polysilicon, but this must be a "single step" deposition for each layer which is not disclosed by applicant in the specification (see arguments on page 2 of amendment filed 8-30-96, Paper No. 21).

- Claims 82 and 88, possibly by typographical error, are directed to a step of "forming holes by CVD," which is not supported by the specification.

- Claims 6-88 provides for a substrate other than silicon, but it is unclear from the specification what other types of selective deposition are possible with non-silicon substrates.

11. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 3, 5, 6, 8, 10, 12, 15, 17, 20, 23, 27, 41, 47-49, 55, and 66 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

- In the newly added independent claims, applicant has broadened the via metal to be "conductive material." It is unclear how this new limitation differs from a "metal" excepting the intention to be polysilicon. Applicant is required define what is meant by "conductive material" in the claims, keeping the need for enablement of the specification in mind. Polysilicon has only been disclosed for the "patterned" lines (e.g. Ref 7), which could be on the wafer surface or surface of the 1st layer, but a method for a one-step selective deposition of polysilicon into the vias has not been disclosed.

- In claim 5, it is unclear what depositing the metal "by one single step" means. Examiner requests clarification of the selective CVD deposition as "one single step" since the record suggests the "single step" involves changing parameters during the step such as gas flow and composition (see Paper No. 26, bottom of page 3).

- In claim 47, it is unclear where in the process applicant intends to "include a junction layer."

- Claims 3 and 8 state that "the [metal] layer...has substantially equal depth." The meaning is presumably that the holes are filled to equal depth, but the wording is not clear. Correction is required.

***Claim Rejections Based on Recapture***

12. Claims 6-88 are rejected under 35 U.S.C. 251 as being an improper recapture of broadened claimed subject matter surrendered in the application for the patent upon which the present reissue is based. See *Hester Industries, Inc.* v. *Stein, Inc.*, 142 F.3d 1472, 46 USPQ2d 1641 (Fed. Cir. 1998); *In re Clement,* 131 F.3d 1464, 45 USPQ2d 1161 (Fed. Cir. 1997); *Ball Corp.* v. *United States*, 729 F.2d 1429, 1436, 221 USPQ 289, 295 (Fed. Cir. 1984). A broadening aspect is present in the reissue which was not present in the application for patent. The record of the application for the patent shows that the broadening aspect (in the reissue) relates to subject matter that applicant previously surrendered during the prosecution of the application. Accordingly, the narrow scope of the claims in the patent was not an error within the meaning of 35 U.S.C. 251, and the broader scope surrendered in the application for the patent cannot be recaptured by the filing of the present reissue application.

- Claims 29, 40, 56, and 81 (row 20 of matrix) attempt to remove the limitation requiring the 1st insulating layer to be etched such that the holes "have a tapered upper portion." This limitation was agreed to by Min Xu in a telephone interview with Thomas Bilodeau on Feb. 13, 1997. The record clearly suggests this "tapered" limitation as placing the case in condition for allowance at the time, noting it is the only amendment at allowance and no other "reason for allowance" is provided (see Paper No. 29).

- Claims 12, 17, 20, 23, 31, 32, and 41 (row 19 of matrix) attempt to remove the limitation that all holes in the first layer are "of substantially equal depth." However, applicant has argued that each hole in the plurality of holes of the first layer are all equal in depth "to prevent [overgrowth]" (see page 4, lines 9-10 of amendment filed 2-12-96, Paper No. 18).

- Claims 6-88 (row 7 of matrix) attempt to broaden the substrate material choice from silicon to any semiconductor, but applicant's only disclosed (and enabled) embodiment is for selective deposition of tungsten on silicon.

***Claim Rejections - 35 USC § 102***

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 27, 39, 41, and 66 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Gutierrez ('749). Gutierrez, as described by the examiner in Paper Nos. 19, 22, and 26 of the original prosecution. Gutierrez teaches all of the claim limitations of these independent claims, but applicant argued that Gutierrez does not teach a "one step" deposition of tungsten on the silicon because a "seed" is required. The examiner replied to the argument that Gutierrez teaches silicon as inherently being a seed for selective tungsten deposition

and that a "single step" involving changing gas composition during the step is still a "single step." Applicant teaches that tapering the upper portion of first layer holes can help align the second layer holes, which is a limitation not taught by Gutierrez, but is a limitation added to all independent claims at the time of the original allowance.

Applicant has failed to distinguish applicant's "single step" tungsten deposition from the deposition of tungsten on silicon as taught by Gutteriezz since applicant disclosed nothing about the particulars of the selective deposition. Gutteriezz teaches that when using tungsten, the silicon is a seed, so no seed is necessary, only a changing of gas once the deposition is started, thus a "single step" applies.

The examiner in Paper No. 26 (bottom of page 3) has indicated that changing a gas during a deposition can still be interpreted as "a single step" deposition. Yet, without any discussion of the method of achieving "a single step" and the meaning of such "a single step", applicant has not provided adequate objective evidence that a unique "one step" deposition is part of applicant's invention.

***Allowable Subject Matter***

14. Claims 1-2, and 4 are allowed.

15. Claim 3 is objected to for a typographical error, but could be allowed if corrected.

16. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record (Gutierrez) fails to teach a step of flaring (tapering) the upper part of the openings in the first layer such that alignment of the holes in the

second layer is achieved more easily. Gutierrez does speak of making the holes narrower for alignment, but this is directed to the device surface (col. 3., lines 44-50). With applicant's improvement of tapering the upper portion of the holes in the 1st layer (referred to in col. 3, line 32 and shown in Fig. 2), tighter spacing of nodes below the 1st layer can be achieved because of the narrower lower portions of the funnel-shaped vias.

***Conclusion***

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Evan T. Pert whose telephone number is 703-306-5689. The examiner can normally be reached on M-F (7:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Bowers can be reached on 703-308-2417. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ETP
March 1, 2000

Charles Bowers
Supervisory Patent Examiner
Technology Center 2800

Charles Bowers
Supervisory Patent Examiner
Technology Center 2800

Serial Number 09/434,736
Art Unit 2813

# APPENDIX TO OFFICE ACTION (Paper No. 6)

MATRIX OF LIMITATIONS vs. CLAIMS

* Claim 66 Preamble = "A semiconductor device..." (See NOTE at end of matrix)

| CLAIM LIMITATIONS | Independent Claim Number 1 | 5 | 6 | 10 | 12 | 15 | 17 | 20 | 23 | 27 | 30 | 31 | 32 | 34 | 36 | 39 | 41 | 66* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1. Preamble: Method to fill contact holes with metal by 2-step metal deposition process | x | x | | | | | | | | | | | | | | | | |
| 2. Preamble: Method of forming a substrate with contact holes | | | x | x | | | | | | | | | | | | | | |
| 3. Preamble: Method of forming a **substrate** with contact holes filled by multi-step deposition of conductive layers | | | | | x | | | | | | | | | | | | | |
| 4. Preamble: Method of forming a **semi-conductor** with contact holes filled by multi-step deposition of **conductive** layers | | | | | | x | x | x | x | x | | | | | | | x | |
| 5. Preamble: Method of forming a **semi-conductor** with contact holes filled by multi-step deposition of **metal** layers | | | | | | | | | | | x | x | x | x | x | x | | |
| 6. provide substrate | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x |
| 7. substrate is silicon | x | x | | | | | | | | | | | | | | | | |
| 8. form oxide (e.g. field oxide) | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x |
| 9. form junction layer or "1st and 2nd regions" | x | x | x | x | x | | | x | x | x | x | | | x | x | x | | 72 |
| 10. form gate electrode | x | x | x | x | | x | | | | x | | x | | | | x | | |
| 11. form "1st conductive pattern" | | | | | | | x | x | | | | | x | x | | | x | x |

NOTE: x = limitation in <u>independent</u> claim
72 = limitation in <u>dependent</u> claim 72

# APPENDIX TO OFFICE ACTION (Paper No. 6)

MATRIX OF LIMITATIONS vs. CLAIMS continued 2 of 5

| CLAIM LIMITATIONS | Independent Claim Number | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| form 1st insulating layer on exposed portions of: | 1 | 5 | 6 | 10 | 12 | 15 | 17 | 20 | 23 | 27 | 30 | 31 | 32 | 34 | 36 | 39 | 41 | 66* |
| 12. the oxide layer | x | x | x | x | x | x | | x | x | x | x | x | x | x | x | x | x | x |
| 13. the junction layer | x | x | x | x | x | | | x | | x | x | | | x | x | x | | |
| 14. the gate electrode (or "conductive pattern") | x | x | x | x | | x | x | x | | x | | x | x | x | | x | x | x |
| 15. form 1st plurality of contact holes | x | x | x | x | **13** | x | | x | x | x | x | x | x | x | x | x | | x |
| 16. form 1st contact hole to expose junction layer and/or 1st conductive pattern | | | | | x | | x | x | | | x | | x | | | | x | |
| 1st plurality of contact holes or "the hole" exposes: | | | | | | | | | | | | | | | | | | |
| 17. junction layer(s) (or "1st and/or 2nd regions) | x | x | x | x | | | | | x | x | | | | x | x | x | | **80** |
| 18. gate electrode(s) or conductive pattern | x | x | x | x | | x | | | | x | | x | | x | x | x | x | x |
| 19. 1st contact holes of substantially equal depth | x | x | x | x | | x | | | | x | x | | | x | x | x | | x |
| 20. 1st contact holes have tapered upper portion | x | x | x | x | x | x | x | x | x | **29** | x | x | x | x | x | **40** | **56** | **81** |
| 21. fill 1st contact holes with 1st material layer | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x |
| 22. form (1st or 2nd) "conductive material" layer into the holes, "entirely" | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | |
| 23. first layer is "metal" and is filled into the holes, "entirely" | x | x | | | | | | | | | x | x | x | x | x | x | | |

# APPENDIX TO OFFICE ACTION (Paper No. 6)

MATRIX OF LIMITATIONS vs. CLAIMS continued 3 of 5

| CLAIM LIMITATIONS | Independent Claim Number | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 5 | 6 | 10 | 12 | 15 | 17 | 20 | 23 | 27 | 30 | 31 | 32 | 34 | 36 | 39 | 41 | 66* |
| 24. fill 1st layer "by one single step" | | x | | | | | | | | | | | | | | | | |
| 25. fill 1st layer in holes "in a continuous step" | | | | x | | | | | | | | | | | | | | |
| 26. 1st layer is grown over and "extends slightly beyond" first plurality of contact holes | x | x | x | x | | | | | | | | | | | | | | |
| 27. form a conductive pattern on 1st insulating layer spaced from 1st metal layer (and/or spaced from 1st conductive material layer) | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x |
| 28. form a "second conductive pattern" | | | | | | | | | | | | | | x | | | x | x |
| form 2nd insulating layer on exposed portions of the: | | | | | | | | | | | | | | | | | | |
| 29. the conductive layer pattern on 1st insulating layer | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x |
| 30. the first insulating layer | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x |
| 31. the 1st plurality of holes or single hole | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x |
| 32. form 2nd plurality of holes in second insulating layer or single hole | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x |
| 33. 2nd plurality of holes are of substantially equal depth | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x |

# APPENDIX TO OFFICE ACTION (Paper No. 6)

MATRIX OF LIMITATIONS vs. CLAIMS continued 4 of 5

| CLAIM LIMITATIONS | Independent Claim Number | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 5 | 6 | 10 | 12 | 15 | 17 | 20 | 23 | 27 | 30 | 31 | 32 | 34 | 36 | 39 | 41 | 66* |
| 2nd plurality of holes formed by removing portions of 2nd insulating layer to expose: | | | | | | | | | | | | | | | | | | |
| 34. the first metal layer | x | x | | | | | | | | | x | x | x | x | x | x | | |
| 35. the (2nd) conductive layer pattern | x | x | x | x | | x | x | x | x | x | x | x | x | x | x | x | x | |
| 36. the (1st) conductive material layer | | | x | x | x | x | x | x | x | x | | | | | | | x | |
| fill (or "form into") a 2nd conductive material layer into 2nd plurality of holes to contact: | | | | | | | | | | | | | | | | | | |
| 37. the 1st conductive material layer | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x |
| 38. the conductive pattern layer | x | x | x | x | | x | x | x | x | x | x | x | x | x | x | x | x | x |
| 39. 1st and/or 2nd layer is metal | x | x | | | **14** | **16** | **19** | **21** | **26** | **28** | x | x | x | x | x | x | | **67** |
| 40. 1st and/or 2nd layers by CVD | **2** | | **7** | | | | | | | | | | | | | | **57,63** | **82,88** |
| 41. 2nd metal layer "filled in each of the 2nd plurality of contact holes has substantially equal depth" | **3** | | **8** | | | | | | | | | | | | | | | |
| 42. 1st and 2nd metal layers are tungsten | **4** | | **9** | | | | | | | | | | | | | | **43** | **68** |
| 43. 1st conductive pattern includes gate | | | | | | | **18** | **22** | | | | **33** | | **35** | | | **45** | **69** |
| 44. "1st region" is a junction layer | | | | | | | | | **24** | | | | | | **37** | | | |
| 45. "2nd region" is a gate electrode | | | | | | | | | **25** | | | | | | **38** | | | |

# APPENDIX TO OFFICE ACTION (Paper No. 6)

MATRIX OF LIMITATIONS vs. CLAIMS continued 5 of 5

| CLAIM LIMITATIONS | Independent Claim Number | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 5 | 6 | 10 | 12 | 15 | 17 | 20 | 23 | 27 | 30 | 31 | 32 | 34 | 36 | 39 | 41 | 66* |
| 46. 1st conductive material layer includes metal | | | | | | | | | | | | | | | | | 42 | |
| 47. conductive material layer is polysilicon | | | | | | | | | | | | | | | | | 44 | 71 |
| 48. 1st conductive pattern layer is a gate stack | | | | | | | | | | | | | | | | | 46 | 70 |
| 49. 1st insulating layer includes oxide | | | | | | | | | | | | | | | | | 51 | 76 |
| 50. 2nd insulating layer includes oxide | | | | | | | | | | | | | | | | | 59 | 84 |
| 51. forming holes includes use of photoresist | | | | | | | | | | | | | | | | | 52,60 | 77,85 |
| 52. forming hole(s) includes wet etch | | | | | | | | | | | | | | | | | 53,61 | 78, 86 |
| 53. forming hole(s) includes dry etch | | | | | | | | | | | | | | | | | 54,62 | 79, 87 |
| 54. junction layer includes "P+" doping | | | | | | | | | | | | | | | | | 49 | 74 |
| 55. junction layer includes "N+" doping | | | | | | | | | | | | | | | | | 48 | 73 |
| 56. 1st conductive pattern layer includes polysilicon | | | | | | | | | | | | | | | | | 50 | 75 |
| 57. 2nd conductive pattern layer includes polysilicon | | | | | | | | | | | | | | | | | 58 | 83 |

*NOTE : Claim 66 is a device claim with comparable limitations (i.e. in this case e.g. "forming a layer" = "having a layer") "Product by Process" claims such as claim 78 do not carry the necessary significant patentable weight, but rather the claims drawn to the device's structure itself. Dependent claim 11 is not included above, but simply defines that in "forming" the conductive material layer, holes are "filled" which is inherent to practice of the invention disclosed. Claims 47 and 55 are not included above, but simply state that the substrate can have a junction over which a hole in the first layer is opened.